a5 upon input control signals and how the data is shared among the logic gates as determined by connections of shared data lines.--

Replace the paragraph beginning at page 5, line 3, with the following rewritten paragraph:

--The shifted data output 16, 19, 22, and 25 may include a plurality of data outputs for each logic gate 11-14. For example, this implementation may be used for dual rail Domino CMOS logic, which produces two outputs for each logic gate, a high output and a a6 complementary low output. Other types of logic gates may likewise implement the data sharing in a multiplexer.--

Replace the paragraph beginning at page 10, line 18, with the following rewritten paragraph:

--Accordingly, use of data sharing consistent with the present invention provides for the elimination of transistors within each logic gate and a savings in area and power consumption on an integrated circuit chip implementing the logic gates. Although two stages a7 of shifting have been shown, different numbers of stages may be used. The number of stages and use of a multiplexer using logic circuit 10 may depend upon a particular application, and performing an FMAC operation is only one such example.--

Replace the paragraph beginning at page 16, line 1, with the following rewritten paragraph:

--Data sharing among adjacent logic gates for shifting data in a multiplexer. Each logic gate implements two stages of shifting and provides for data sharing by connecting data a8 inputs among the logic gates. Based upon the data sharing connections, control signals feed bits into each logic gate from adjacent logic gates to perform various shifting operations on a data bus.--

IN THE CLAIMS:

Amend claims 1 and 11 as follows:

1. (Amended) A logic circuit for use in a multiplexer to shift data, comprising:

a plurality of logic gates, each logic gate receiving data inputs and control signals, wherein each data input uses a single transistor; and

a9 a plurality of shared data lines connecting the logic gates, the shared data lines interfacing through a transistor on each of the logic gates to provide a portion of the data inputs for each of the logic gates by connecting data inputs among the plurality of logic gates,

wherein the logic gates shift data received at the data inputs by one or more data bits based upon the control signals and the connections of the shared data lines, and wherein each of the logic gates receives one data input using the single transistor for the data input and receives other data inputs from the plurality of shared data lines.

a10 11. (Amended) A method of using a multiplexer to shift data, comprising: